REMARKS

Entry and favorable action of the claims are earnestly solicited in light of the above amendments.

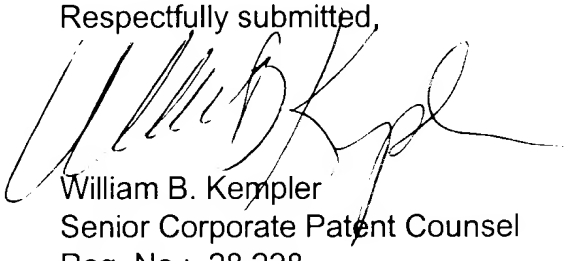
Applicants have amended the claims inter alia to avoid multiple dependent claims and to place the claims in the appropriate form.

Early action on the merits is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current preliminary amendment. The attached page is captioned **"Version with markings to show changes made."**

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) An insulation film for providing an insulation substrate for carrying a semiconductor chip of a semiconductor package[; wherein] comprising:

two rows of sprocket holes [are provided] comprising a plurality of sprocket holes formed at a pitch L along both edges of the insulation film;

a plurality of through holes is formed two-dimensionally at a pitch p between the rows of sprocket holes; and

the plurality of through holes [can be used] for use selectively as through holes for the insulation substrate of the semiconductor package according to size of the semiconductor package.

2. (Amended) The insulation film according to claim 1[;] wherein the pitch L and the pitch p satisfy the following equation: m p = n L (i.e.,] wherein n and m are integers that satisfy the equation n < m[)].

3. (Amended) The insulation film according to claim 1 [or claim 2;] wherein the insulation film [has the following] comprises:

a plurality of circuit patterns formed two-dimensionally upon the insulation film according to size of the semiconductor package; and

a for-plating-electricity-supply-use conductor pattern electrically connected with the plurality of circuit patterns.

4. (Amended) The insulation film according to claim 3[;] wherein the for-plating-electricity-supply-use conductor pattern [has the following] comprises:

a main line surrounding [the] a perimeter of the plurality of circuit patterns; and

a sub-line electrically connecting each of the circuit patterns to the main line.

5. (Amended) A method for manufacture of an insulation film for providing an insulation substrate for carrying a semiconductor chip of a semiconductor package comprising the steps of:

[preparing] providing an insulation film having two rows of sprocket holes comprising a plurality of sprocket holes formed at a pitch L along both edges of the insulation film; and

forming a plurality of through holes two-dimensionally at a pitch p between the rows of sprocket holes.

6. (Amended) The method for manufacture of an insulation film according to claim 5[;] wherein the pitch L and the pitch p satisfy the following equation: m p = n L [(i.e.,] wherein n and m are integers that satisfy the equation n < m[)].

7. (Amended) The method for manufacture of an insulation film according to claim 6[;] wherein the step of forming the through holes further comprises the steps of:

forming the through holes by collective punching out at the effective sprocket hole formation width of the through holes along the transverse direction of the insulation film in a region of length n L along the length-wise direction of the insulation film;

moving the insulation film [just] a length n L in the length-wise direction by means of the sprocket holes; and

repeating these two steps alternately.

8. (Amended) The method for manufacture of an insulation film according to claim 6 [or claim 7;] wherein the method further comprises a step of forming a plurality of circuit patterns two-dimensionally upon the insulation film according to size of the semiconductor package and a for-plating-electricity-supply-use conductor pattern electrically connected with the plurality of circuit patterns.

9. (Amended) A method for manufacture of a semiconductor package comprising the steps of: [preparing] providing an insulation film, [having the following:] forming two rows of sprocket holes comprising a plurality of sprocket holes formed at a pitch L along both edges of the insulation film, forming a plurality of through holes [formed] two-dimensionally at a pitch p

between the rows of sprocket holes, forming a plurality of circuit patterns [formed] two-dimensionally upon the insulation film according to size of the semiconductor package, forming a for-plating-electricity-supply-use conductor pattern electrically connected with the plurality of circuit patterns having a main line surrounding [the] a perimeter of the plurality of circuit patterns and a sub-line electrically connecting each of the circuit patterns to the main line;

mounting [of] a semiconductor chip within a respective prescribed region of each circuit pattern of the insulation film and electrically connecting the semiconductor chip[s] with the circuit pattern[s];

performing resin sealing for partitioning off each region enclosed by the main line of the conductor pattern; and

cutting apart into individual semiconductor packages by dicing along the sub-lines of the insulation film.

10. (Amended) The method for manufacture of a semiconductor package according to claim 9[;] wherein the method further comprises [a] the step of plating each of the circuit patterns upon the insulation film using the for-plating-electricity-supply-use conductor pattern.

11. (Amended) The method for manufacture of a semiconductor package according to claim 9 [or claim 10;] wherein the [above mentioned] dicing step is carried out by use of a dicing blade having a blade trim width wider than the wiring width of the sub-line of the conductor pattern [so that] whereby the sub-line is not left behind upon the insulation film.

Please add new claims 12-13 as follows:

--12. (New) The method for manufacture of an insulation film according to claim 7 wherein the method further comprises a step of forming a plurality of circuit patterns two-dimensionally upon the insulation film according to size of the semiconductor package and

a for-plating-electricity-supply-use conductor pattern electrically connected with the plurality of circuit patterns.

13. (New) The method for manufacture of a semiconductor package according to claim 10 wherein the dicing step is carried out by use of a dicing blade having a blade trim width wider than the wiring width of the sub-line of the conductor pattern whereby the sub-line is not left behind upon the insulation film.--